## REMARKS

Claims 1-9 and 12-13 are pending in this application. The Examiner rejected Claims 1-9 under 35 U.S.C. §112, first paragraph, rejected under 35 U.S.C. §102(b), and withdrew Claims 12 and 13 from further consideration as being drawn to nonelected species. The foregoing amendment amends independent Claim 1 and withdraws Claims 12 and 13. No claims have been previously allowed.

## Claim Rejections – 35 U.S.C. §112

Claims 1-9 were rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. In particular, the Examiner contended that the phrase "metallurgical contact" did not exist within the specification. The phrase "metallurgical contact" is understood to those in the field of semiconductor technology to mean region to region contact, such as a pn junction. Figure 2 shows the claimed region to region contacts and thus, the claim is supported by the specification. Nevertheless, Claim 1 has been amended to more clearly define the region to region contacts between the claimed semiconductor regions. Accordingly, it is requested that this rejection be withdrawn.

## *Jambotkar* Does Not Anticipate the Invention of Claims 1-9

Claims 1-9 were rejected under 35 U.S.C. 102(b) as anticipated by U.S. Patent No. 4,264,857 to Jambotkar ("*Jambotkar*"). This rejection is traversed for the reasons discussed below.

### Claim 1

The semiconductor device of Claim 1 requires a first semiconductor region of a first conductivity type, defined by an upper end surface, a lower end surface opposing to the upper end surface, and first and second side boundary surfaces connecting the upper and lower end surfaces when viewed in section; a second semiconductor region of the first

conductivity type disposed under the first semiconductor region and being in contact with said first semiconductor region so as to have the lower end surface as a common tangent plane between the first and second semiconductor regions; a third semiconductor region of a second conductivity type disposed on the first semiconductor region and being in contact with said first semiconductor region so as to have the upper end surface as a common tangent plane between the first and third semiconductor regions; and a fourth semiconductor region having first and second inner surfaces in contact with the first and second side boundary surfaces respectively when viewed in section and an impurity concentration lower than said first semiconductor region, configured such that the fourth semiconductor region is disposed between the second and third semiconductor regions.

The Examiner contended that *Jambotkar* teaches a device comprising a first semiconductor region of a first conductivity type, defined by an upper end surface and a side boundary surface connecting the upper and lower end surfaces when viewed in section (Fig. 2A (16)); a second semiconductor region of the first conductivity type in metallurgical contact (s1) with the first semiconductor region at the lower end surface (Fig. 2A (14)); a third semiconductor region of a second conductivity type in metallurgical contact (B1) with the first semiconductor region at the upper end surface (Fig. 2A(12)); and a fourth semiconductor region having inner surface in metallurgical contact (W1) with the side boundary surface when viewed in section and an impurity concentration lower than the first semiconductor region, configured such that the fourth semiconductor region is disposed between the second and third semiconductor regions (Fig. 2A (10)).

In *Jambotkar* the second semiconductor region of the first conductivity type 14 is neither disposed under the first semiconductor region 16 nor in contact with the first semiconductor region 16 so as to have the lower end surface as a common tangent plane between the first and second semiconductor regions. Figure 2A of *Jambotkar* illustrates that the second semiconductor region 14 of *Jambotkar* is used as a source region and the first

semiconductor region 16 is used as a drain region of a field effect transistor (Column 2, lines 21-24). The second semiconductor region 14 contacts electrically with the first semiconductor region 16 through an electrical connection such as surface wiring. The region underneath the gate oxide layer 18 comprises the surface portion of third semiconductor region 12 and forms the channel region 20 between the source region 14 and the drain region 16 (Column 2, lines 34-36). *Jambotkar* fails to disclose a second semiconductor region of the first conductivity type disposed under the first semiconductor region and being in contact with said first semiconductor region so as to have the lower end surface as a common tangent plane between the first and second semiconductor regions, as recited in Claim 1.

Moreover, *Jambotkar* fails to disclose a third semiconductor region of a second conductivity type disposed on the first semiconductor region and being in contact with the first semiconductor region so as to have the upper end surface as a common tangent plane between the first and third semiconductor regions. In *Jambotkar*, the first semiconductor region 16 is buried in the third semiconductor region 12 such that the first semiconductor region 16 and the third semiconductor region 12 have a common top surface, as shown in Fig. 2A. Thus, the third semiconductor region 12 of *Jambotkar* is not disposed on the first semiconductor region 16, nor is the third semiconductor region 12 in contact with the first semiconductor region 16 so as to have the upper end surface of the first semiconductor region as a common tangent plane between the first and third semiconductor regions.

*Jambotkar* further fails to disclose a fourth semiconductor region having inner surface being in contact with the side boundary surface of the first semiconductor region, configured such that the fourth semiconductor region is disposed between the second and third semiconductor regions. In *Jambotkar*, the fourth semiconductor region 10 is in contact with the bottom surface of the third semiconductor region 12. The inner surface of the fourth semiconductor region 10 never contacts the side boundary surface of the first semiconductor region 16, as shown in Fig. 2A. Moreover, the fourth semiconductor region 10 of *Jambotkar*

is not disposed between the second semiconductor region 14 and the third semiconductor region 12, as shown in Fig. 2A.

Accordingly, amended Claim 1 is not anticipated by *Jambotkar*. The Applicants submit that amended Claim 1 should be allowed.

**Claims 2-9**

Claims 2-9 depend either directly or indirectly from amended Claim 1. The remarks made above in support of the patentability of independent Claim 1 are equally applicable in distinguishing dependent Claims 2-9 from *Jambotkar*. Accordingly, Claims 2-9 should also be allowed.

## CONCLUSION

The foregoing is submitted as a complete response to the Office Action identified above. This application should now be in condition for allowance, and the Applicant solicits a notice to that effect. If there are any issues that can be addressed via telephone, the Examiner is asked to contact the undersigned at 404.685.6799.

Respectfully submitted,

Brenda O Holmes

By: Brenda O. Holmes
Reg. No. 40,339

KILPATRICK STOCKTON LLP
1100 Peachtree Street
Suite 2800
Atlanta, Georgia 30309-4530
(404) 815-6500
Our Docket: 44471-267680